

PERFORMANCE ANALYSIS OF THIRTY-ONE LEVEL MULTILEVEL INVERTER FOR ELECTRIC VEHICLE APPLICATION

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Abstract

This research provides a new architecture for reduced component count 31-level multilevel inverter (MLI). The suggested design uses four unequal DC sources and an H-bridge to provide a maximum 31-level output voltage. For applications using renewable energy, the topology designed for the 31-level can be employed. This lowers the system's total cost, number of components, and size. Higher level counts for lower total harmonic distortion (THD), however, dependability concerns are more significant than MLIs' many benefits. Total standing voltage (TSV), cost function (CF), and power loss are the various metrics that are examined for 31-level MLI. Experiments with different combinational loads and dynamic load fluctuations with sudden load disturbances are performed to assess the inverter's performance. The cost-effectiveness of the suggested MLI is demonstrated while comparing its TSV with the cost function against other topologies that have been recently published.

Key words: multilevel inverter, nearest level control, cost function, total standing voltage, total harmonic distortion, pulse width modulation

Introduction. Multilevel inverters have drawn attention recently owing to their high-power operating capabilities and other advantages, including enhanced electromagnetic interference reduction, higher power quality, reduced harmonics, and fewer switching losses. These MLIs use a diversity of DC sources and power

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electronic circuitry made up of power components to generate a stepped voltage waveform at their output [1, 2]. Three types of MLIs are typically distinguished: Diode Clamped MLI (DCMLI), Flying Capacitor MLI (FCMLI), and Cascaded H-bridge MLI (CHMLI). Circuit management becomes increasingly difficult with DCMLI because it requires more diodes and a larger number of components as the output waveform's levels rise. By utilizing the redundancy in switching schemes given by the capacitors, the voltage balance issue in DCMLI can be addressed in FCMLI; nevertheless, a higher number of passive circuit components would impair circuit dependability [3–6]. In contrast to these topologies, CHMLI is far more modular and controllable. Additionally, since it requires independent DC sources, the requirement for balancing circuits is avoided. However, in a typical CHMLI, each extra DC voltage source increases the requirement for four electronic power switches. Researchers are now looking toward higher-level inverter topologies known as reduced element count MLI setups with fewer power devices since standard circuits require more power devices [7, 8]. Due to their special features, multilevel inverters are becoming more and more common in a range of average to high-voltage, high-power applications [9–12]. The hybrid multi-conversion cell and H-bridge concepts are combined in the suggested 31 level inverter to produce both positive and negative polarity. The primary design feature of the recommended configuration has fewer components.

Proposed 31 level inverter. Figure 1 depicts the general setup of a recommended topology for MLI. This inverter is composed of one H-bridge and one multi conversion cell. In multi-conversion cell, four voltage sources (V_{DC1} , V_{DC2} , V_{DC3} , V_{DC4}) are linked to one another by a circuit that consists of a switch and a diode. It can only produce positive stepped output voltage with 31 levels. Four power switches are linked with H-bridge configuration to create the alternate polarity in nature. The first level of resultant voltage $+1V_{dc}$ is attained by switching on the power switches S_1 (S_2 , S_3 and S_4 are turned off). The identical approach can be used to reach additional levels by activating the relevant power switches at predetermined intervals, as depicted in Table 1. The 'P' DC voltage sources and the corresponding output levels can be determined using the equation below:

$$(1) \quad N_{level} = 2^{P+1} - 1.$$

As an example, if the value of $P = 4$, the resulting waveform will have 31 steps or stages ($0, \pm 1V_{dc}, \pm 2V_{dc}, \pm 3V_{dc}, \pm 4V_{dc}, \pm 5V_{dc}, \pm 6V_{dc}, \pm 7V_{dc}, \pm 8V_{dc}, \pm 9V_{dc}, \pm 10V_{dc}, \pm 11V_{dc}, \pm 12V_{dc}, \pm 13V_{dc}, \pm 14V_{dc}$ and $\pm 15V_{dc}$). Moreover, the equation provided can be used to evaluate the resultant output at each level

$$(2) \quad V_{DCP} = 2^{P-1} V_{dc} \quad (P = 1, 2, 3, \dots).$$

This configuration's power switch count for producing single-phase voltage can be found using the following equation:

$$(3) \quad N_{switch} = P + 4 \quad (P = 1, 2, 3, \dots).$$

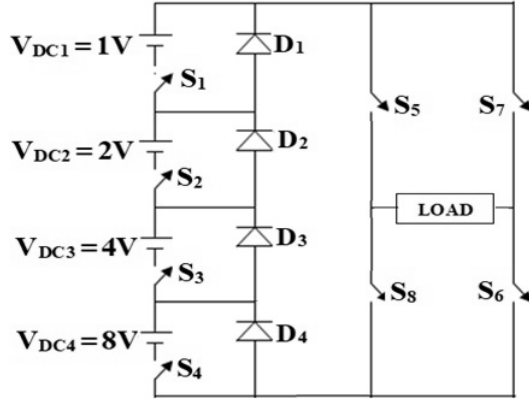


Fig. 1. Configuration of the suggested 31 level inverter

Estimation of loss and efficiency. In the suggested inverter, power switches are used as a unit for polarity conversion, and the load current in a single phase is measured in relation to the neutral. In this case, the loss resulting from the switches' conduction period during the basic cycle's quarter is calculated.

$$(4) \quad P_{CON} = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} I_{RP}^2(t) R_{ON} T dt.$$

The transistor's ON-state resistance and load current are denoted by $R_{on}T$ and $I_{RP}(t)$, respectively. The load current can be written as

$$(5) \quad I_{RP} I_{PP} \sin \omega t.$$

The average loss of the single-phase system during conduction is determined by applying (4) and (5) as shown below:

$$(6) \quad P_{CON1} = \frac{4}{\pi} \int_0^{\frac{\pi}{2}} I_{PP}^2 \sin^2 \omega t R_{ON} T dt.$$

One MOSFET switch for the multi-conversion portion is on during the fundamental period. The multi-conversion loss for the period of π is as follows:

$$(7) \quad P_{CON2} = \frac{1}{\pi} \int_0^{\pi} I_{PM}^2 \sin^2 \omega t R_{ON} T dt.$$

The diode's conduction losses in the single leg of a multi-conversion cell are provided by

$$(8) \quad P_{CD}(t) = [V_{DP} + R_{DP} i(t)] i(t).$$

R_{DP} is the diode equivalent resistance and V_{DP} is the diode voltage drop in the forward path.

T a b l e 1

Switching configuration of 31 level multilevel inverter

S. No	Intervals	S ₁	S ₂	S ₃	S ₄	D ₁	D ₂	D ₃	D ₄	Output voltage (Volt)
1	I	0	0	0	0	OFF	OFF	OFF	OFF	0 V
2	II	1	0	0	0	OFF	ON	ON	ON	15 V
3	III	0	1	0	0	ON	OFF	ON	ON	30 V
4	IV	1	1	0	0	OFF	OFF	ON	ON	45 V
5	V	0	0	1	0	ON	ON	OFF	ON	60 V
6	VI	1	0	1	0	OFF	ON	OFF	ON	75 V
7	VII	0	1	1	0	ON	OFF	OFF	ON	90 V
8	VIII	1	1	1	0	OFF	OFF	OFF	ON	105 V
9	IX	0	0	0	1	ON	ON	ON	OFF	120 V
10	X	1	0	0	1	OFF	ON	ON	OFF	135 V
11	XI	0	1	0	1	ON	OFF	ON	OFF	150 V
12	XII	1	1	0	1	OFF	OFF	ON	OFF	165 V
13	XIII	0	0	1	1	ON	ON	OFF	OFF	180 V
14	XIV	1	0	1	1	OFF	ON	OFF	OFF	195 V
15	XV	0	1	1	1	OFF	ON	ON	ON	210 V
16	XVI	1	1	1	1	OFF	OFF	OFF	OFF	225 V
17	XVII	0	1	1	1	OFF	ON	ON	ON	210 V
18	XVIII	1	0	1	1	OFF	ON	OFF	OFF	195 V
19	XIX	0	0	1	1	ON	ON	OFF	OFF	180 V
20	XX	1	1	0	1	OFF	OFF	ON	OFF	165 V
21	XXI	0	1	0	1	ON	OFF	ON	OFF	150 V
22	XXII	1	0	0	1	OFF	ON	ON	OFF	135 V
23	XXIII	0	0	0	1	ON	ON	ON	OFF	120 V
24	XXIV	1	1	1	0	OFF	OFF	OFF	ON	105 V
25	XXV	0	1	1	0	ON	OFF	OFF	ON	90 V
26	XXVI	1	0	1	0	OFF	ON	OFF	ON	75 V
27	XXVII	0	0	1	0	ON	ON	OFF	ON	60 V
28	XXVIII	1	1	0	0	OFF	OFF	ON	ON	45 V
29	XXIX	0	1	0	0	ON	OFF	ON	ON	30 V
30	XXX	1	0	0	0	OFF	ON	ON	ON	15 V
31	XXI	0	0	0	0	OFF	OFF	OFF	OFF	0 V

The power losses of the diode in the multi-conversion cell is provided by

$$(9) \quad P_{CON3} = \frac{1}{2\pi} \int_0^{2\pi} N_{DM}(t) P_C D(t) dt.$$

Multi-conversion unit in the projected MLI, the loss during conduction is

attained as given below:

$$(10) \quad P_{CON-TOTAL} = P_{CON1} + P_{CON2} + P_{CON3}.$$

When a MOSFET switches from ON to OFF state, or vice versa, the overlying voltage and current cause switching losses. The following formula is used to determine the energy loss of MOSFET power switches during their on and off times:

$$(11) \quad E_{ON} = \frac{V_{ON} \times I}{6} T_{ON},$$

where V_{ON} , I , T_{ON} are the MOSFET voltage during ON state, the MOSFET current after ON and OFF period, respectively.

$$(12) \quad E_{OFF} = \frac{V_{OFF} \times I}{6} T_{OFF}.$$

V_{OFF} , I_{OFF} , and T_{OFF} are the MOSFET voltage during OFF state, current travelling through the MOSFET before ON and OFF period, respectively. The average loss in the projected configuration is estimated using equations (11) and (12) and is determined independently for power switches in each unit. The switching loss in polarity conversion unit is calculated as follows:

$$(13) \quad P_{SW1} = 2 \times f \times (E_{ON} + E_{OFF}) = \frac{1}{3} \times f \times I \times (V_{ON}T_{ON} + V_{OFF}T_{OFF}).$$

The fundamental switching frequency is f . Similarly, during the half period, the switching loss of multi-conversion unit is given as

$$(14) \quad P_{SW2} = 2 \times f \times (E_{ON} + E_{OFF}) f \times I (V_{ON}T_{ON}V_{OFF}T_{OFF}).$$

The switching losses of the diode in the multiconversion unit is given as

$$(15) \quad P_{SW3} = \frac{1}{2} C_R \times V_R^2 \times f_{sw} + \frac{1}{6} I_{RR} * V_R \times t_b \times f_{sw}.$$

For a full cycle, the overall switching loss can be deduced as

$$(16) \quad P_{SW-TOTAL} = f \times (P_{SW1} + P_{SW2} + P_{SW3}).$$

The losses of the projected inverter are determined by using (17)

$$(17) \quad P_{LOSS,,TOTAL} = P_{CON,T} + P_{SW,T}.$$

The efficiency of the suggested configuration has been calculated using the following formula:

$$(18) \quad \text{Efficiency} = \frac{P_{OUT}}{P_{out} + P_{LOSS,T}} \times 100\%.$$

Nearest level control technique for 31 level inverter. NLC is a common approach used in modular multilevel converters. Low switching frequency control technology known as NLC or the round approach is adaptable and simple to use. The semiconductor switches of the converter are activated by the appropriate gating signals produced by the NLC approach. Take the basic sinusoidal function with unit magnitude multiplied by the modulation index as a starting point. Allow the resulting signal to pass through the inverter's total positive levels (N) after that. Employ the round function next to obtain the necessary levels. The round function serves to effectively decrease switching losses by causing just one commutation to occur between two voltage steps, as shown in Fig. 2. Considering a V_{ref} , the modulation index 'm' the nearest voltage level can be estimated as follows:

$$V_{ref} = \mu \left(\frac{L-1}{2} \right) V \sin(wt) = V_m \sin(wt) V_{ref},$$

$$m = \frac{V_m}{\left(\frac{L-1}{2} \right) V}, \quad V_m = V_{round} \left(\frac{V_{ref}}{V} \right).$$

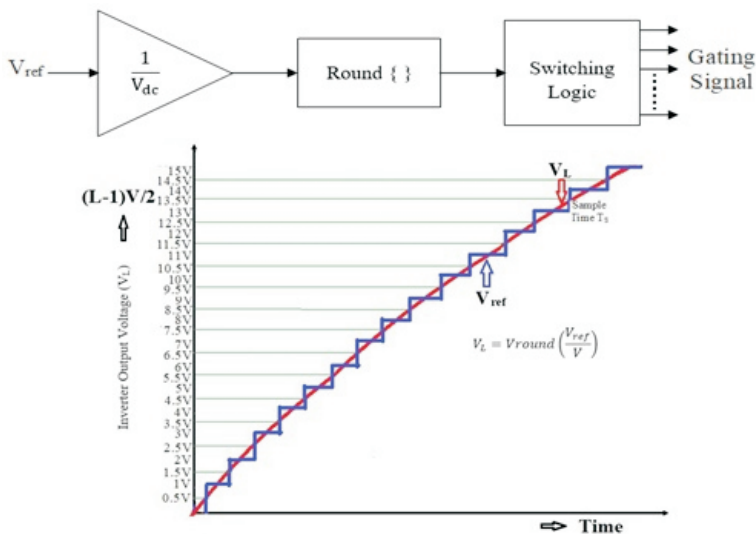


Fig. 2. NLC technique synthesis for 31 level inverter

Figure 2 pronounces the identification of the nearest voltage level and the principle of NLC method for the projected 31 level inverter.

Results and discussion. The magnitude of pulses is 1 V for switches $S_1, S_2, S_3, S_4, S_5, S_6, S_7, S_8$ for proposed 31 level inverter. Figure 3(a) and (b) represents the voltage and current waveform for resistive load of 100Ω , the magnitude of rms voltage waveform is 225 V and current value is 2.2 A. Figure 3(c) and (d) denotes the voltage and current waveform for RL load ($R=100 \Omega, L=100 \text{ mH}$). There is no

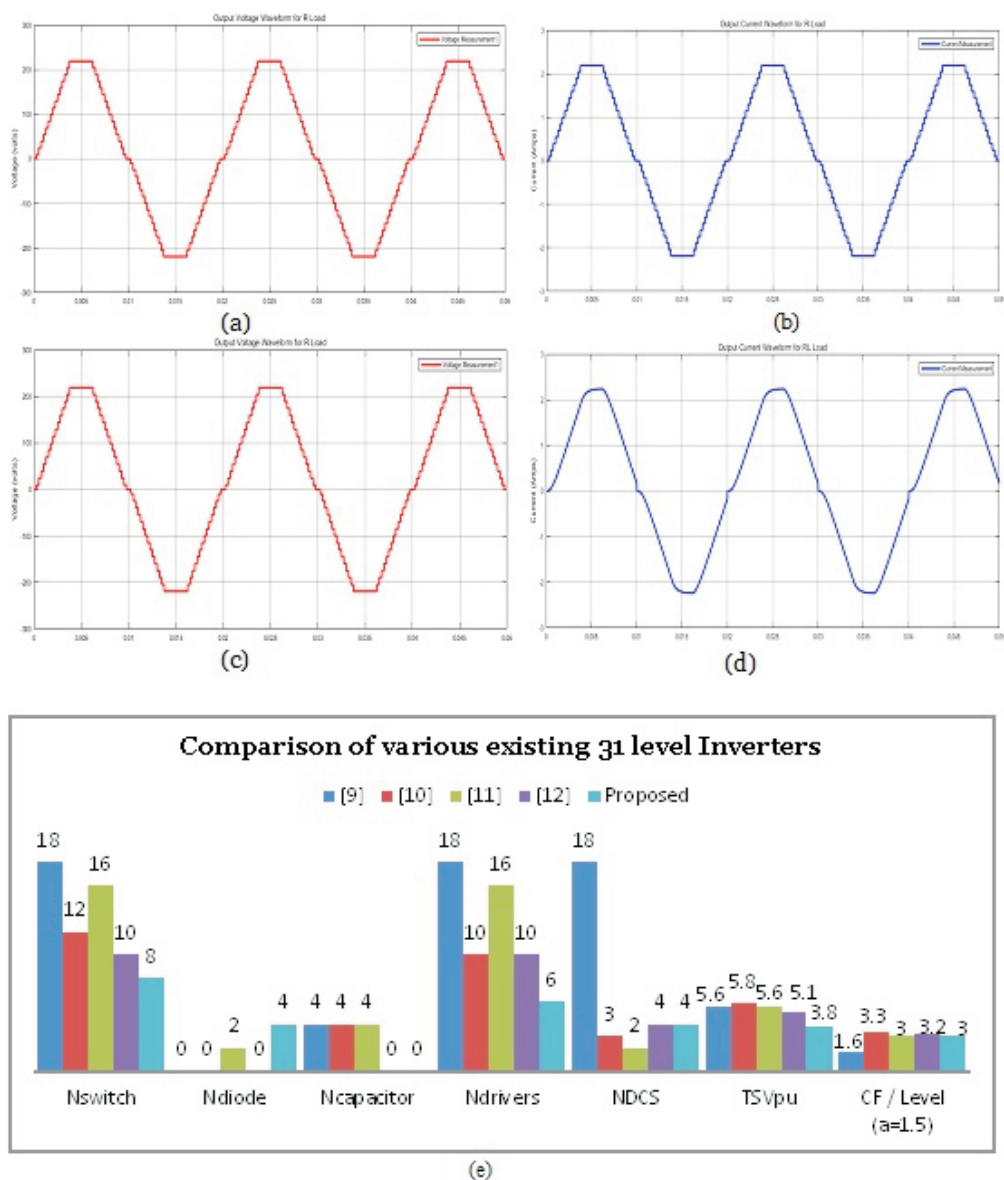


Fig. 3. (a) Output voltage waveform for R load; (b) Current waveform for R load; (c) Voltage waveform for RL load; (d) Current waveform for RL load; (e) Comparison of various parameters

in change in the nature of waveform and its magnitude. The rms value of voltage waveform remains constant and current value is also the same. The nature of the current waveform is smooth and almost sinusoidal. THD produced by this inverter is 3.34%.

The simulation result is validated with the hardware prototype. MOSFETs are used as switching devices and the line to neutral voltage is 180 V. The in-

verter is made up of 8 MOSFET switches. IRF840 MOSFETs are employed in the hardware setup. The gate signal for inverter switches is generated by DSP Processor. In the input side of projected 31-level inverter, four unequal voltage DC sources, 12 V, 24 V, 48 V, and 96 V are deployed. THD of the hardware set up is 3.27%. Figure 3(e) illustrates the comparison made for various 31 level inverters on usage of power elements, diodes, driver circuits, TSV and cost function per level. The CF per level is 2.57 for the weight factor of 0.5 and cost function per level is 3.058 for the weight factor of 1.5. The recommended MLI has benefits of 31 levels with only eight power switches when the multisource is utilized. The comparison results show that the proposed MLI is best suited for electric vehicles with only eight power switches and four diodes. It also yields reduced THD and more efficiency.

Calculation of cost function. The total standing voltage of the projected multilevel inverter is calculated as follows:

$$(20) \quad \text{Total Standing Voltage} = \sum_{i=1}^n MBV_{Si}$$

$$\text{TSV} = \text{MBV}_{S1} + \text{MBV}_{S2} + \text{MBV}_{S3} + \text{MBV}_{S4} + \text{MBV}_{S5} + \text{MBV}_{S6} + \text{MBV}_{S7} + \text{MBV}_{S8}$$

$$\text{TSV} = 13V_{dc} + 10V_{dc} + 4V_{dc} + 0V_{dc} + 7.5V_{dc} + 7.5V_{dc} + 7.5V_{dc} + 7.5V_{dc}$$

$$\text{TSV} = 57V_{dc}$$

$$\text{TSV}_{PU} = \frac{\text{TSV}}{\text{MBV}} = \frac{57V_{dc}}{15V_{dc}} = 3.8 .$$

The cost function of the proposed MLI is calculated by equation (21)

$$(21) \quad \text{CostFunction} = (N_S \text{WT} + N_{\text{Driv}} + N_{\text{Di}} + N_{\text{Cap}} + \alpha \text{TSV}_{PU}) \times N_{\text{DCS}}.$$

Cost function is

$$N_S = 8, N_{\text{Driv}} = 6, N_{\text{Di}} = 4, N_{\text{Cap}} = 0, \alpha = 0.5 \text{ and } N_{\text{DC}} = 4.$$

$$\text{Cost Function} = (8 + 6 + 4 + 0 + 0.5 \times 3.8) \times 4 = 79.6.$$

Cost function per level is calculated as

$$\text{CF/Level} = \frac{\text{CF}}{\text{Number of Levels}} = \frac{79.6}{31} = 2.577.$$

Cost function is

$$N_S = 8, N_{\text{Driv}} = 6, N_{\text{Di}} = 4, N_{\text{Cap}} = 0, \alpha = 1 \text{ and } N_{\text{DC}} = 4.$$

$$\text{Cost Function} = (8 + 6 + 4 + 0 + 1.5 \times 3.8) \times 4 = 87.2.$$

$$\text{CF/Level} = \frac{\text{CF}}{\text{Number of Levels}} = \frac{87.2}{31} = 3.058.$$

Conclusion. The proposed work has validated the structural set up of 31 level inverter. In the conservative approaches, the number of power switches was increased based on levels. Due to the engrossment of large count of power switches, total harmonics distortion, switching losses, and the implementation cost are also increased. The suggested technique diminishes the power switches to 8 for 31 levels which will lessen the losses due to switching, lower order harmonics, cost and leads to reduction in THD. The cost function of the proposed MLI is 3.05 for weight factor 1.5. Hence, the introduced MLI is suitable for electric vehicle applications.

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